A Brief View of the Cell Broadband Engine

Cris Capdevila
Adam Disney
Yawei Hui
Alexander Saites

Overview

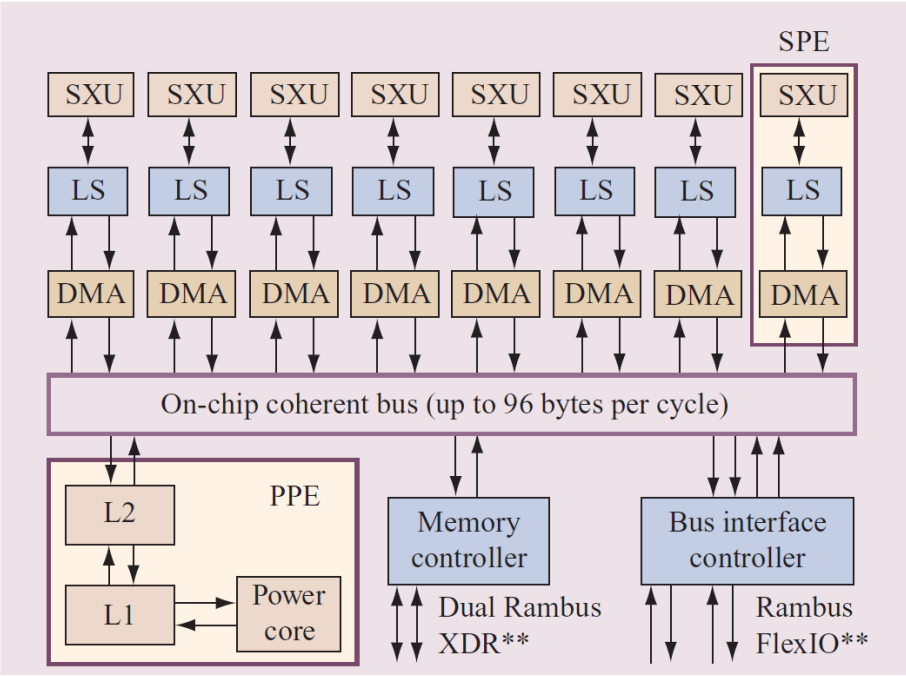
- Brief History
- System Overview
  - Power Processor Element & Cache
  - Synergistic Processing Elements
  - Element Interconnect Bus
- Programming Challenges

Brief History

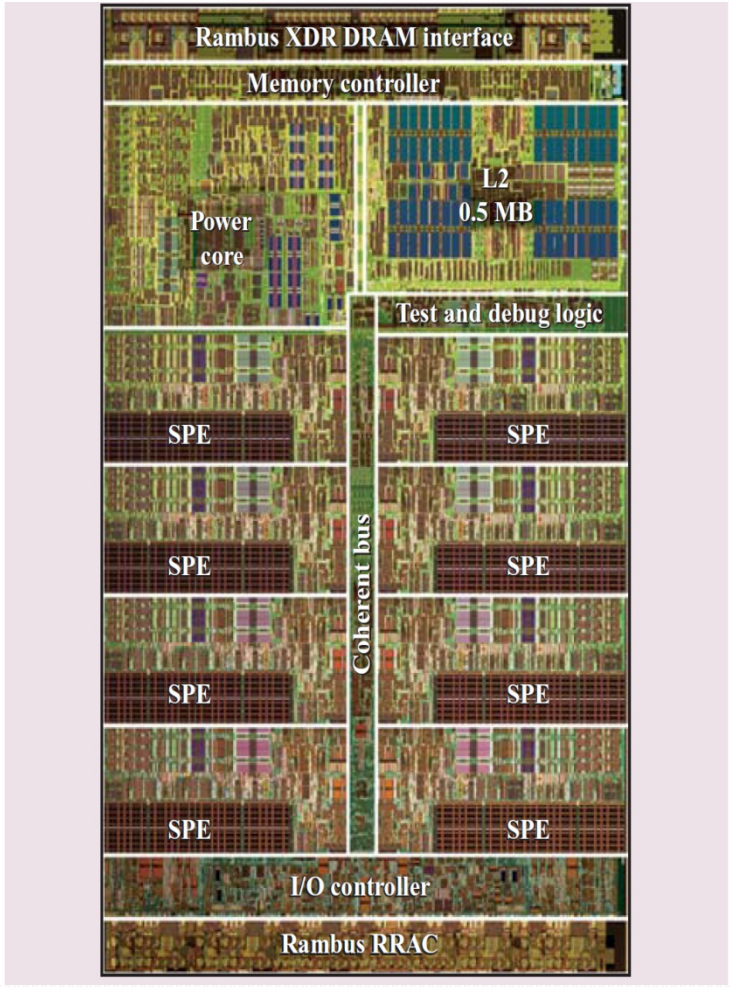
- Developed by STI (Sony, Toshiba, IBM)
- Initially targeted for PS3
- Focus on high data throughput
- In 2008, IBM made the PowerXCell 8i, which lead to Roadrunner

System Overview

- PPE: PowerPC Processor Elements
  - General CPU
  - Handles system management
- SPE: Synergistic Processor Elements
  - Many working together
  - Data-heavy, parallel computation
- EIB: Element Interconnect Bus
  - Ring design
  - Connects SPEs



Block diagram



Die photo

J. A. Kahle et al. (2007), "Introduction to the Cell Multiprocessor", *IBM J. Res. & Dev.*, vol. 49, no. 4-5, pp. 589, July/Sept, 2005.

Power Processor Elements

- Main CPU(s)
- 64-bit compliant core
- Instruction Unit, Execution Unit, and Vector SIMD
- 23-stage pipeline with dual-instruction execution
- 8-bit branch predictor (2-bit local, 6-bit global)
- No dynamic reorder – just dual-issue interleave
  - Vector-Scalar Unit (VSU) splits pipeline

PPE Cache

- Two 32-KB L1 caches (instruction and data)
  - Two-way associative memory
  - 512 wordlines; 32 bytes per way
  - Full clock rate
- One 512-KB L2 cache
  - Includes L1 data cache
  - Half clock rate
  - Energy efficient (only 1/8 activated at a time)
  - Interleaved read/write for continuous data transfer

Synergistic Processing Elements

- Synergistic Processor Unit
  - 128 by 128-bit SIMD registers
  - Inherently SIMD
- Local Store
  - Special 256 KB non-cached local memory
  - Holds both instructions and data
  - SPE local stores isolated from each other
  - Fast 32 bit mailbox registers for communication
- Memory Interface Controller
  - Connects SPEs to other SPEs/PPEs
  - Uses Direct Memory Access (DMA) controller
  - 96 bytes per cycle peak transfer rate

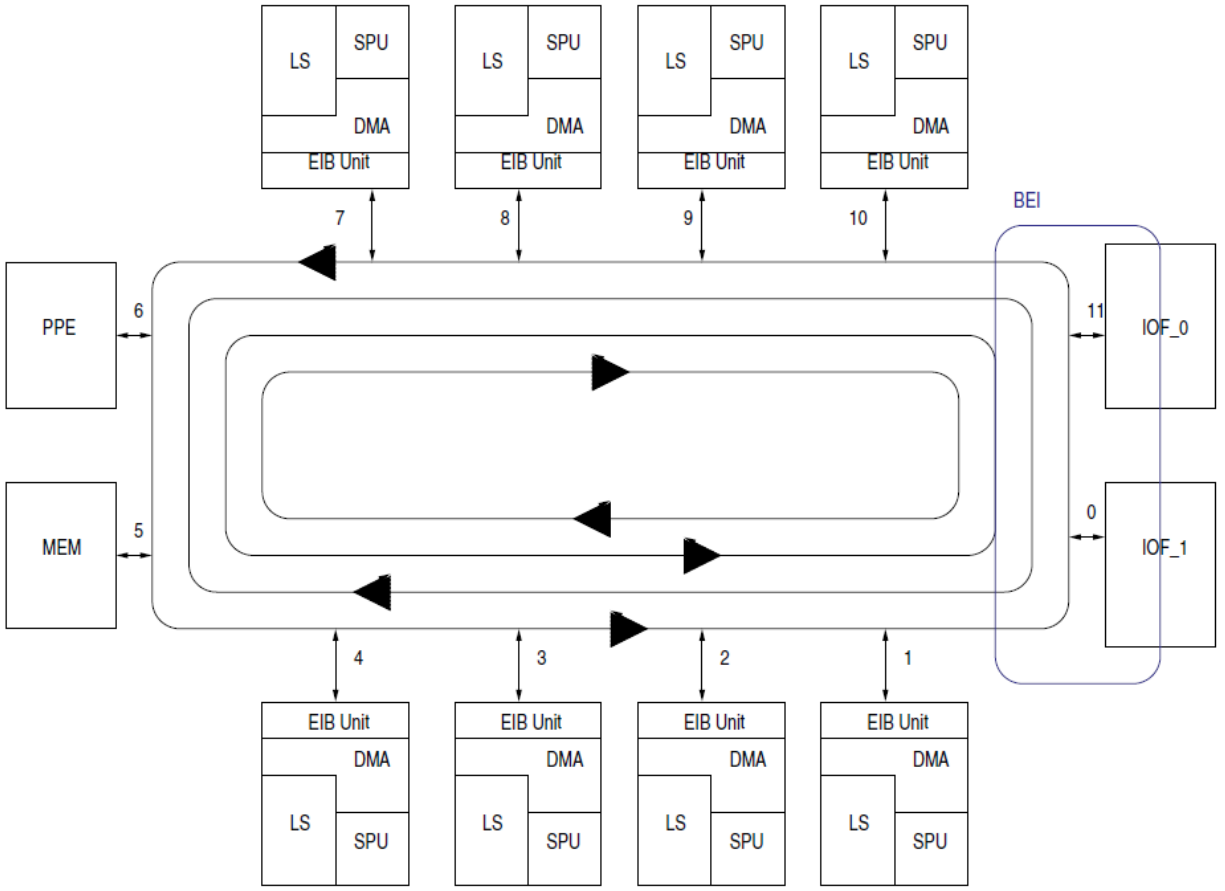
Synergistic Processing Elements

- 23 Stage Pipeline, Dual Issue
  - Integer operations: 2 cycles
  - Float operations: 6 cycles
  - Double precision operations: 7 cycles, single issue
  - No branch prediction
- Memory Interface Controller
  - Connects SPEs to other SPEs/PPEs
  - Uses Direct Memory Access (DMA) controller
  - 96 bytes per cycle peak transfer rate

Element Interconnect Bus

- Connects off-chip memory controllers and I/O
  - Enables memory coherent SMP with other Cell processors
- Token ring-like layout
  - One address bus
  - Four 16 byte wide data rings, 128 bytes per ring
  - Latency between SPEs variable
  - DMA requests have highest priority

Element Interconnect Bus



Programming Challenges

- Parallel Programming is Hard
- Low storage in SPEs
- Efficiency over Ease – burden on programmer
  - SPEs had no cache
  - SPEs had no branch prediction
  - SPEs execute in-order
  - Manual loop-unrolling and function in-lining

Thank You!